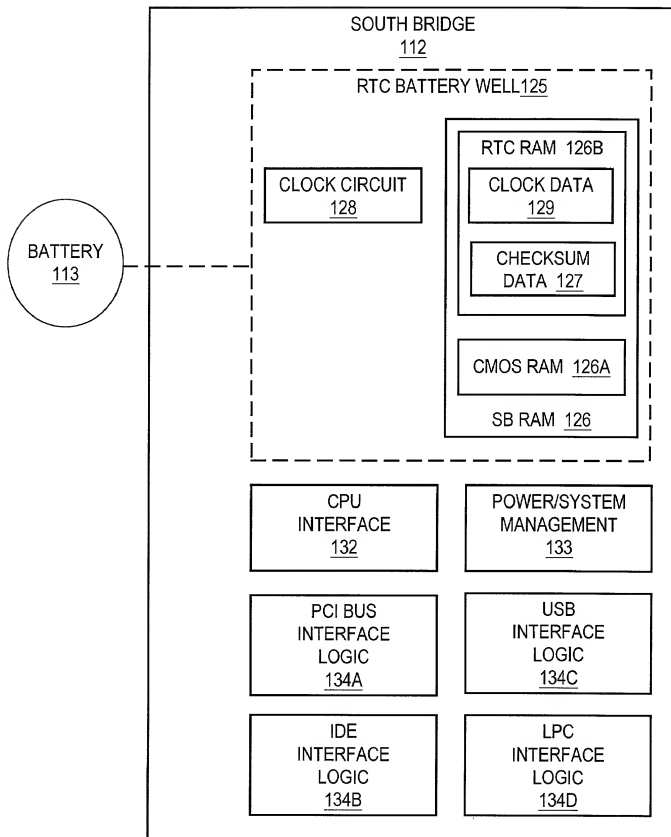


The diagram illustrates a computer system architecture with the following components and connections:

- PROCESSOR 102** is connected to the **NORTH BRIDGE 104**.
- MEMORY 106** is connected to the **NORTH BRIDGE 104**.
- AGP 108** is connected to the **NORTH BRIDGE 104**.
- The **NORTH BRIDGE 104** is connected to the **SOUTH BRIDGE 112** via a vertical bus.
- The **SOUTH BRIDGE 112** is connected to **IDE 114** and **USB 116** via a horizontal bus.
- The **SOUTH BRIDGE 112** is connected to the **PCI 110** bus via a horizontal bus.
- The **SOUTH BRIDGE 112** is connected to the **LPC BUS 118** via a horizontal bus.
- The **SOUTH BRIDGE 112** is connected to the **SUPER I/O 120** and **BIOS 122** via a vertical bus.

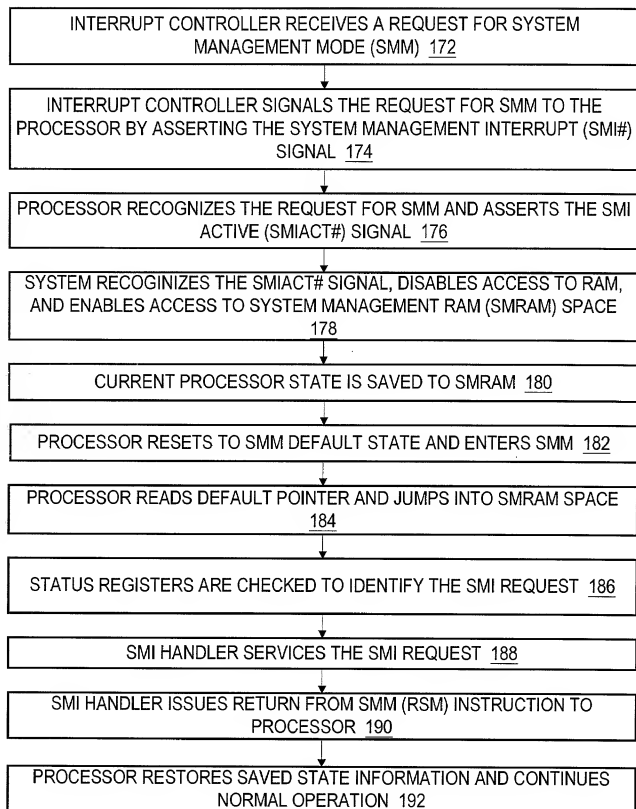
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**Fig. 1B**  
**(Prior Art)**



**Fig. 2A**  
**(Prior Art)**



**Fig. 2B**  
**(Prior Art)**

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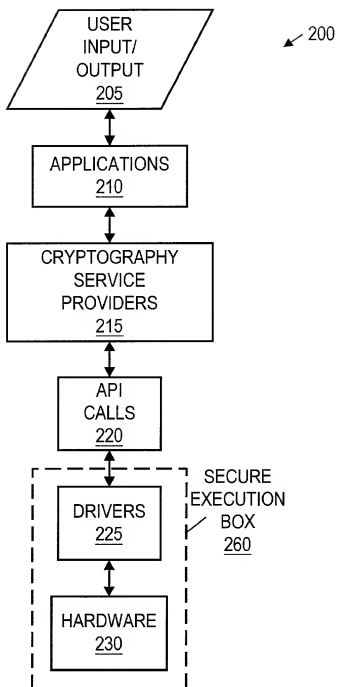


Fig. 3

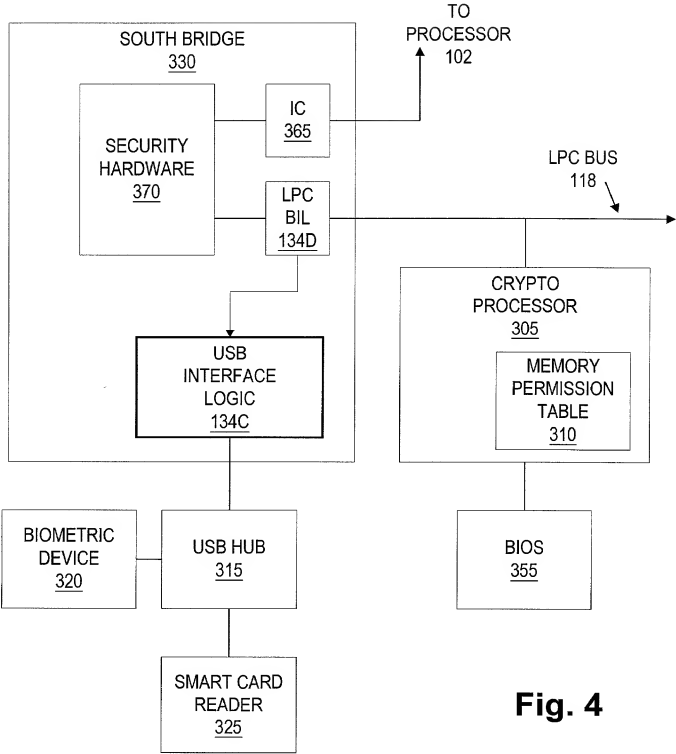
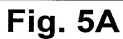


Fig. 4

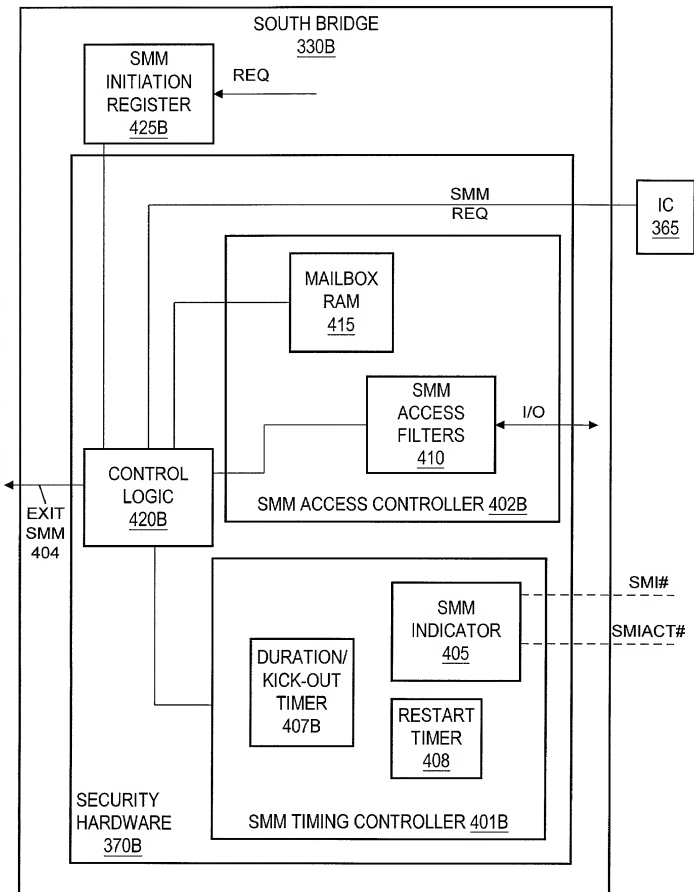
005225-00101



**Fig. 5A**

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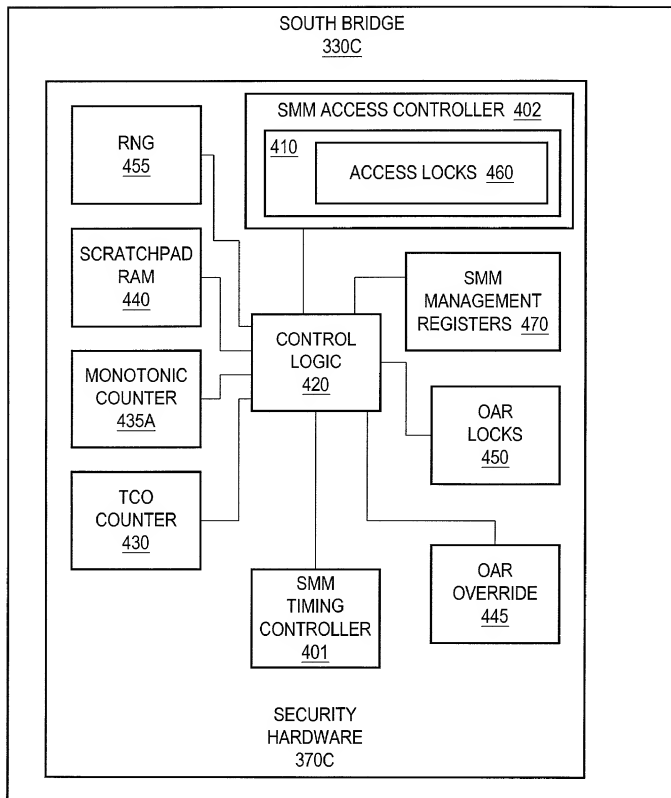
005325.05101  
10150.422580



**Fig. 5B**



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**Fig. 6**

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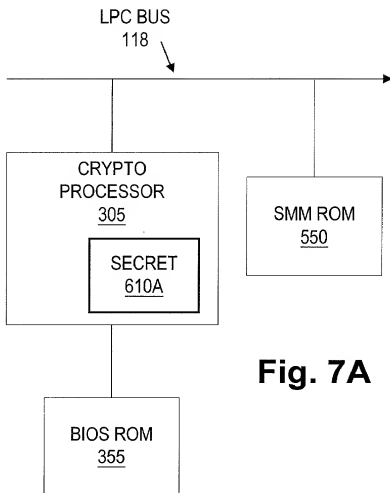


Fig. 7A

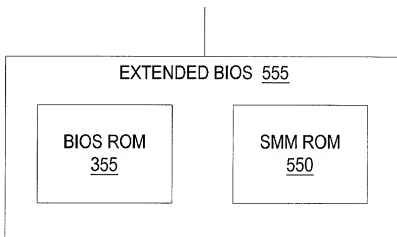
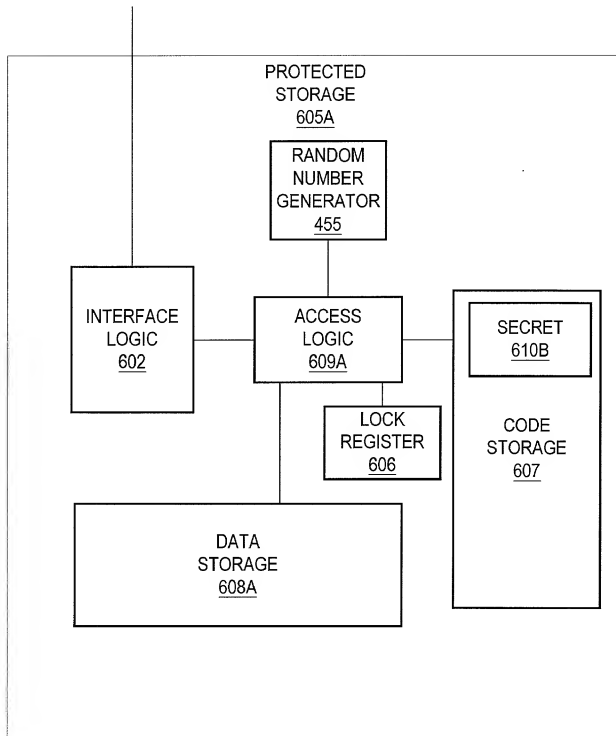


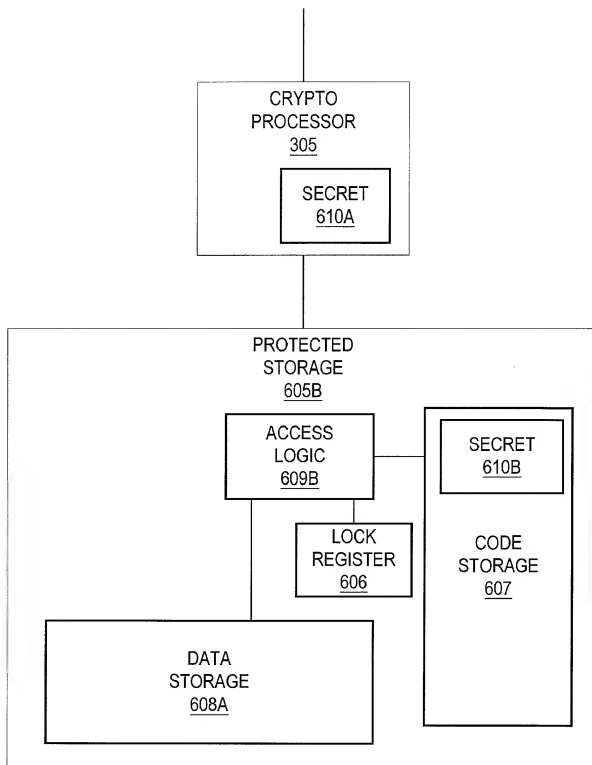
Fig. 7B

00000000-00000000

**Fig. 7C**



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**Fig. 7D**

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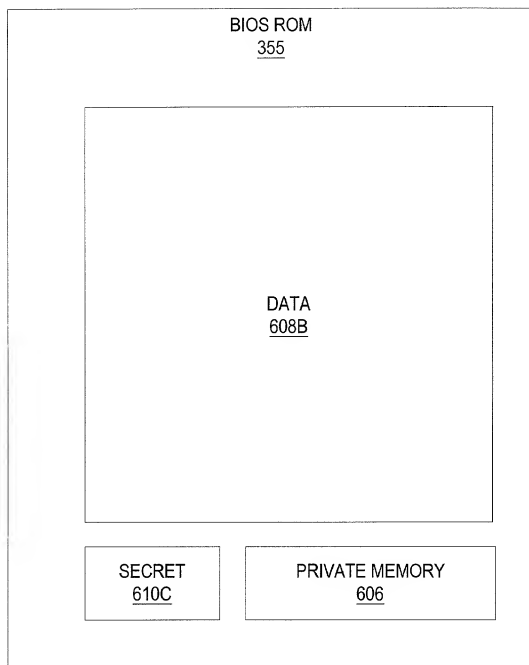


Fig. 8A

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SMM ROM  
550



**Fig. 8B**

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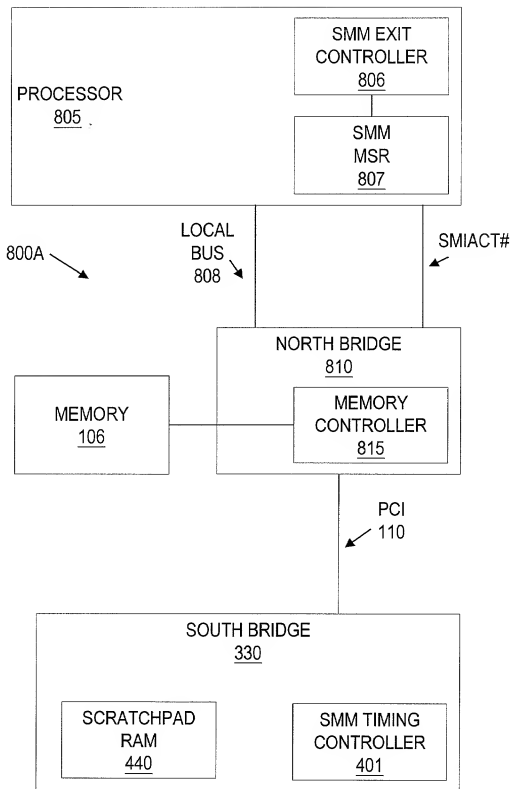
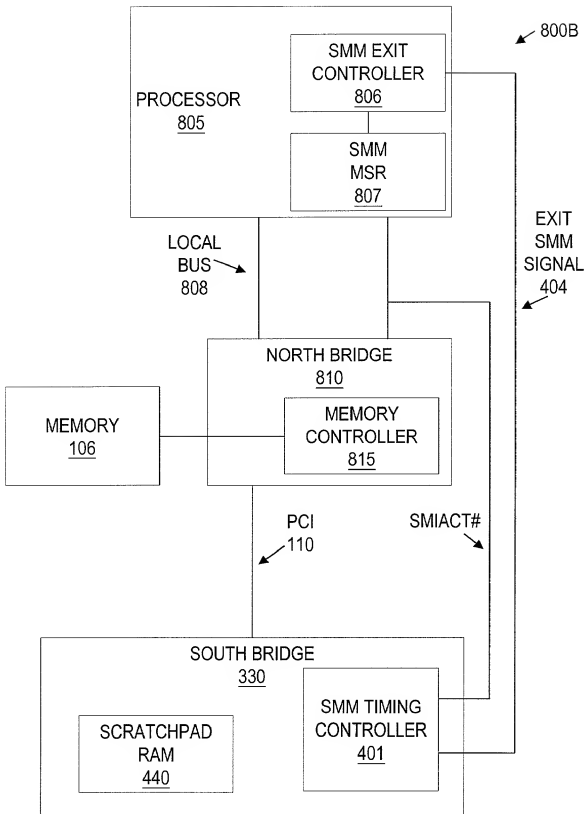


Fig. 9A

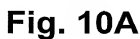
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**Fig. 9B**



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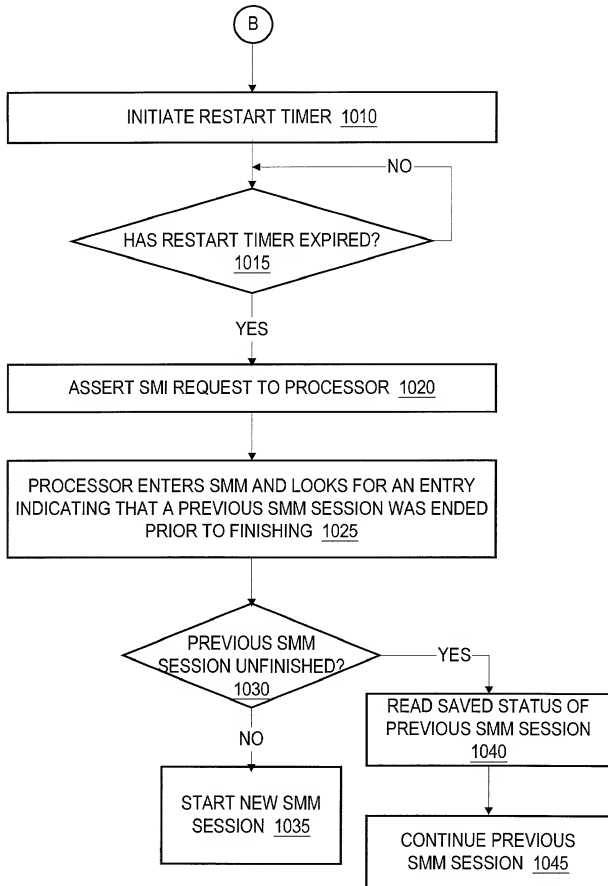


Fig. 10B

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1100A

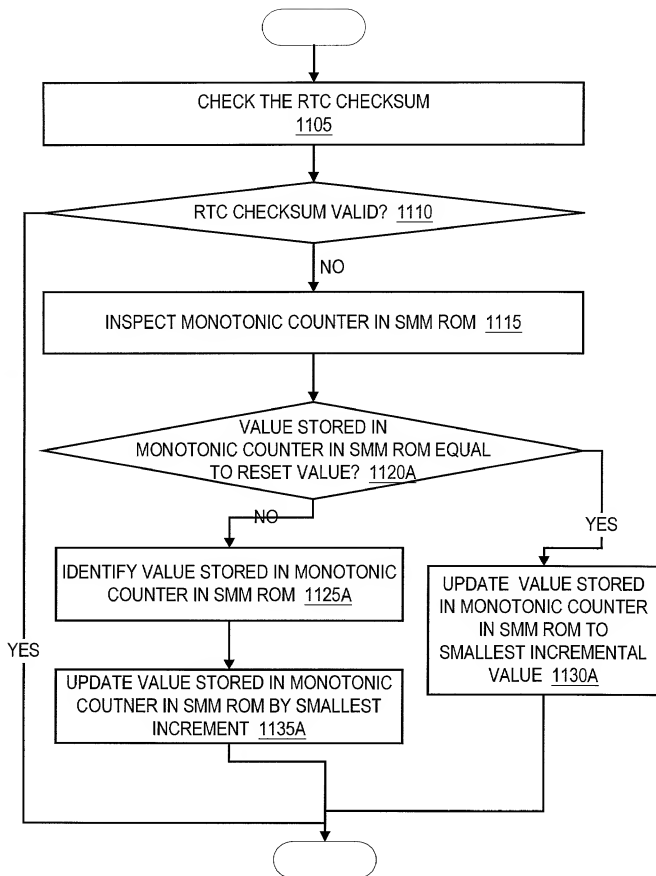


Fig. 11A

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1100B

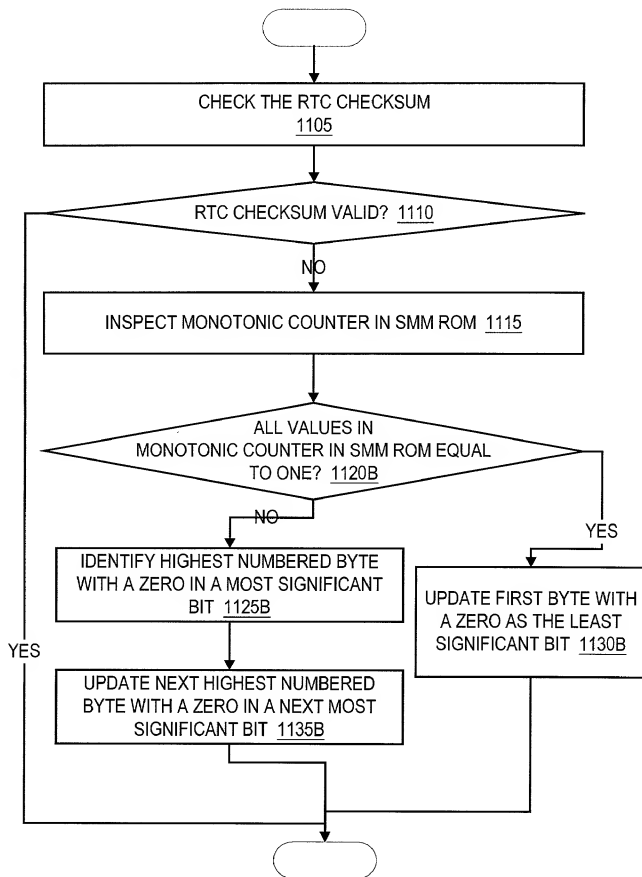


Fig. 11B

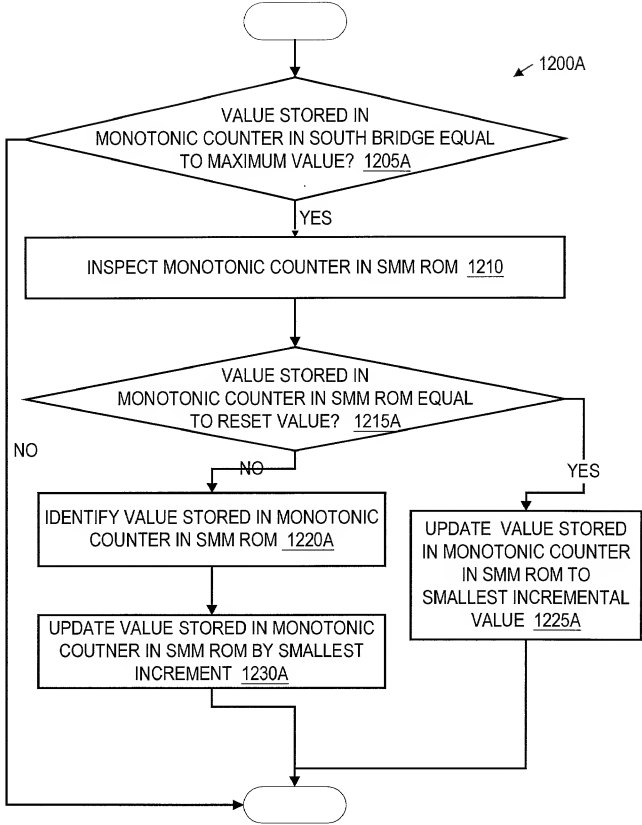


Fig. 12A

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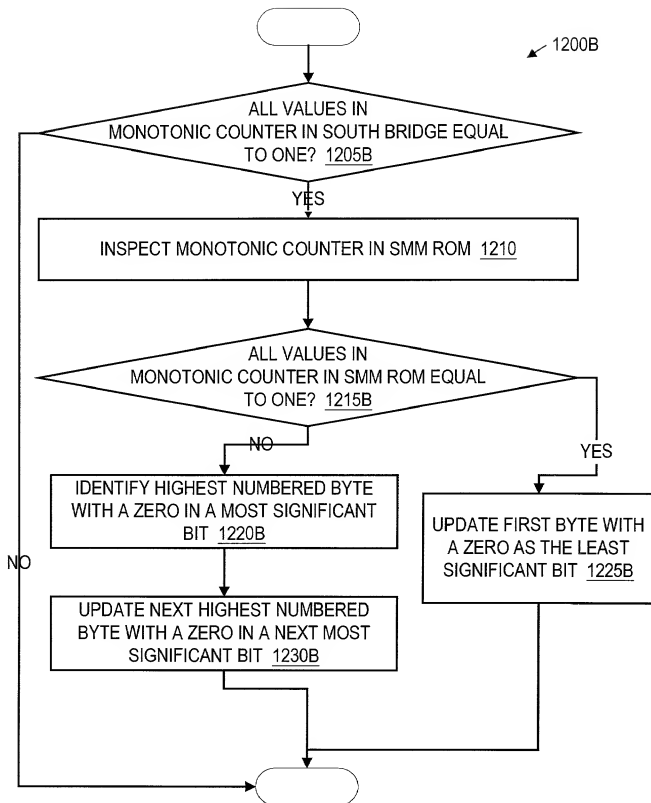


Fig. 12B

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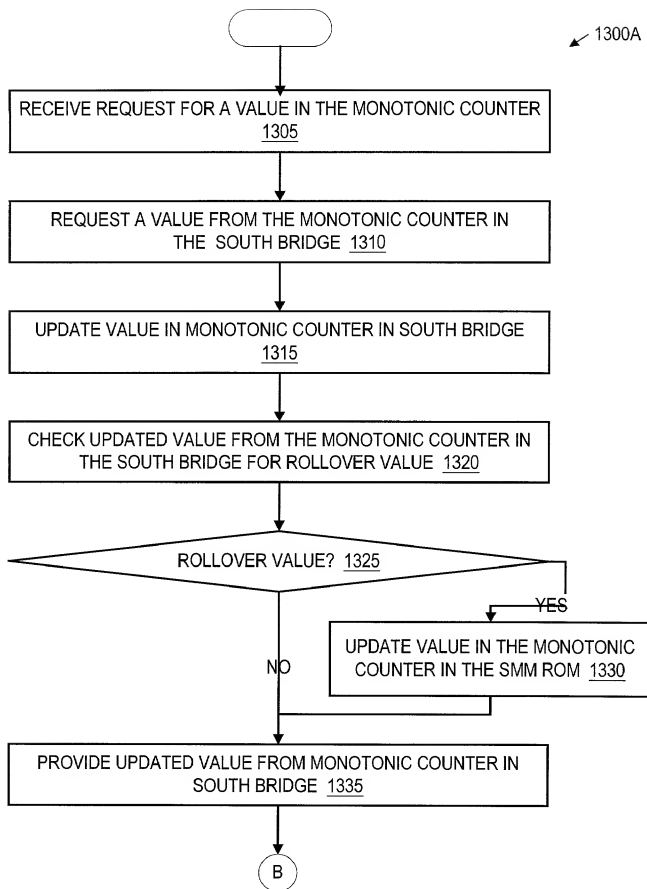


Fig. 13A

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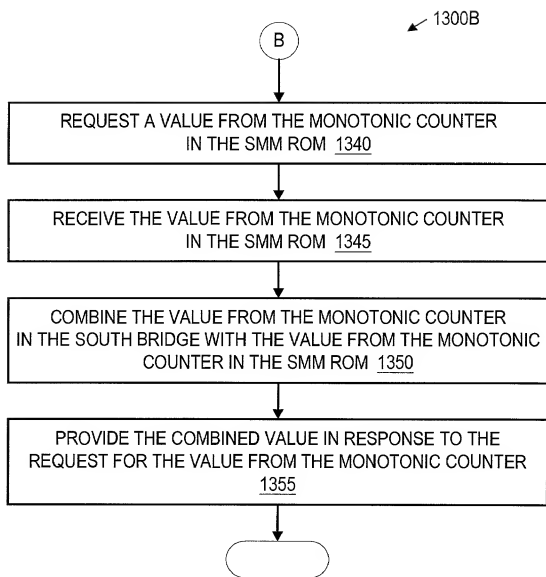


Fig. 13B



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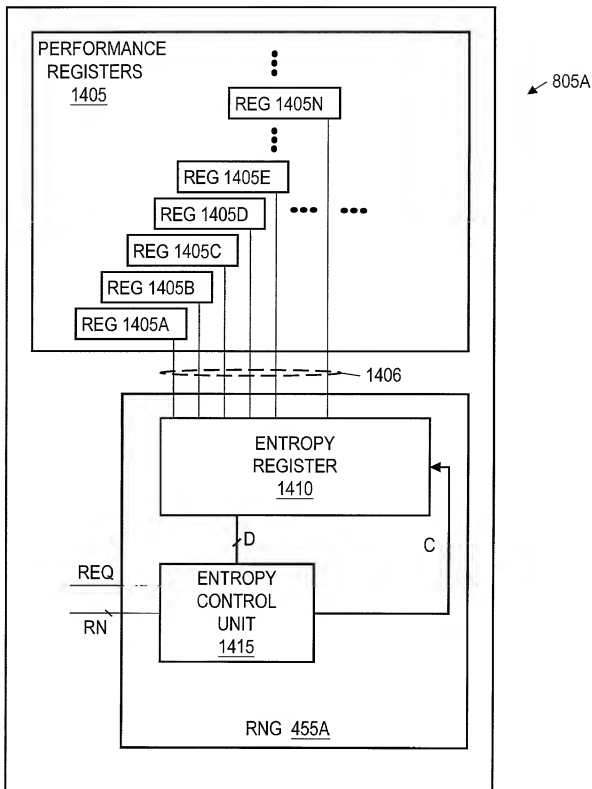


Fig. 14A

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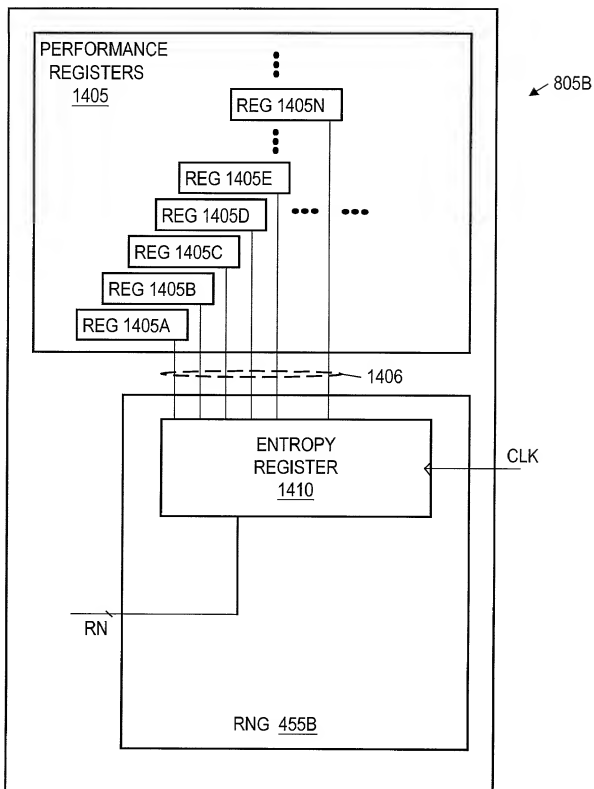


Fig. 14B

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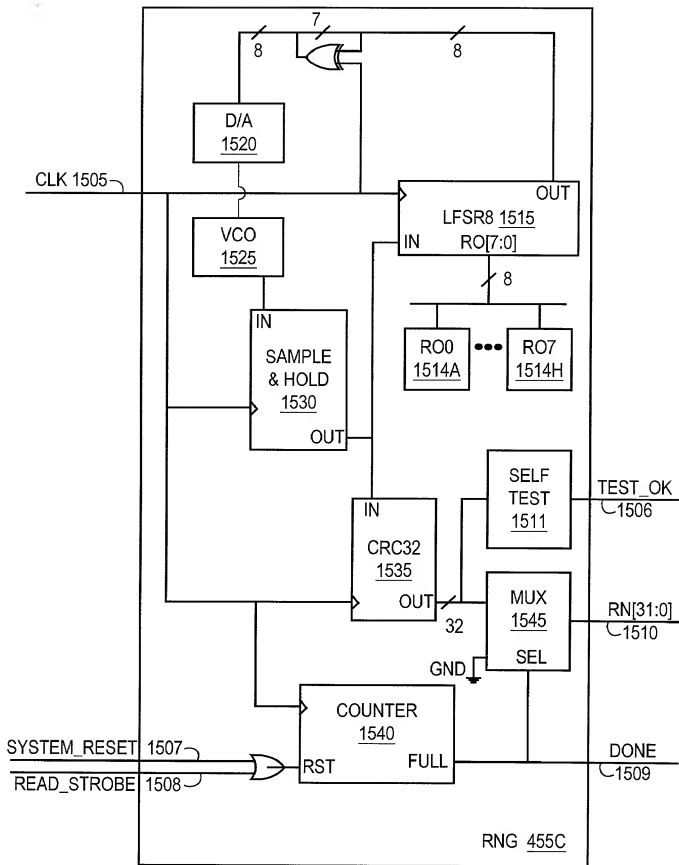


Fig. 15

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1600A

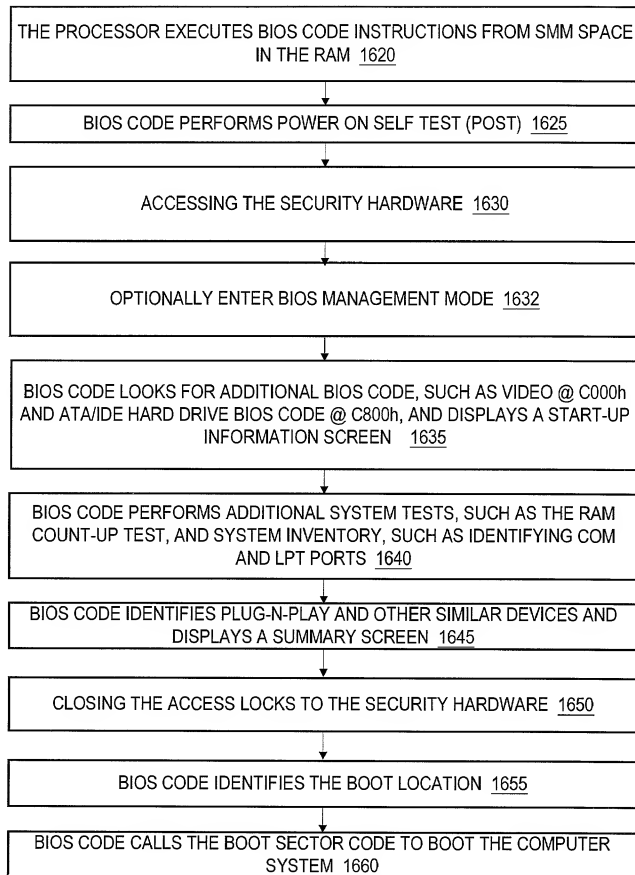


Fig. 16A

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1600B

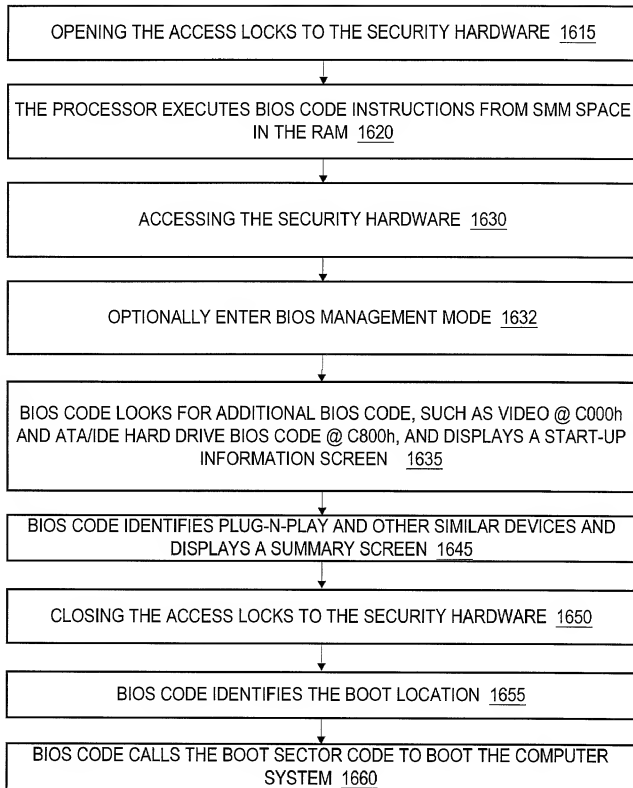


Fig. 16B

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1600C

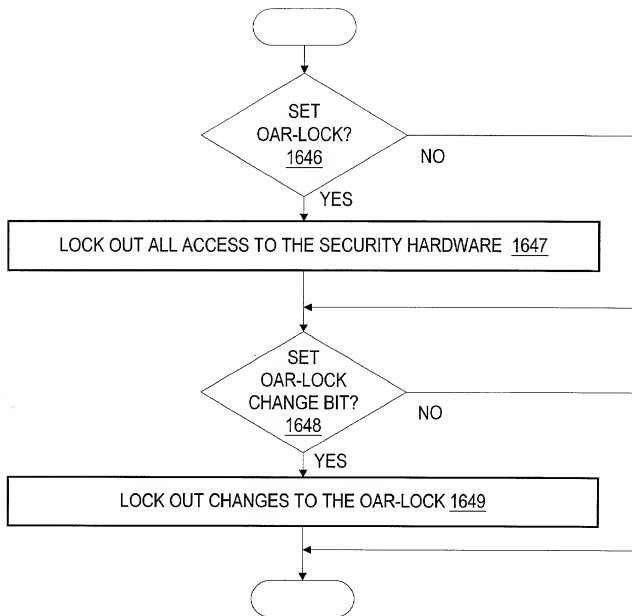


Fig. 16C

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1600D

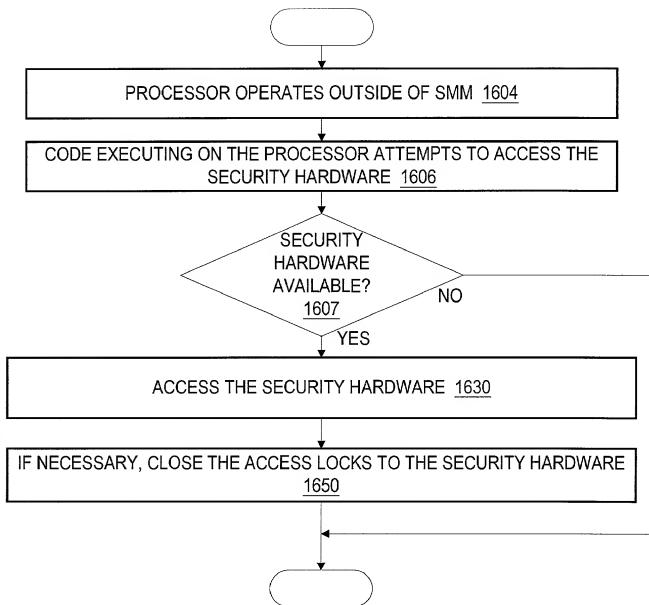


Fig. 16D

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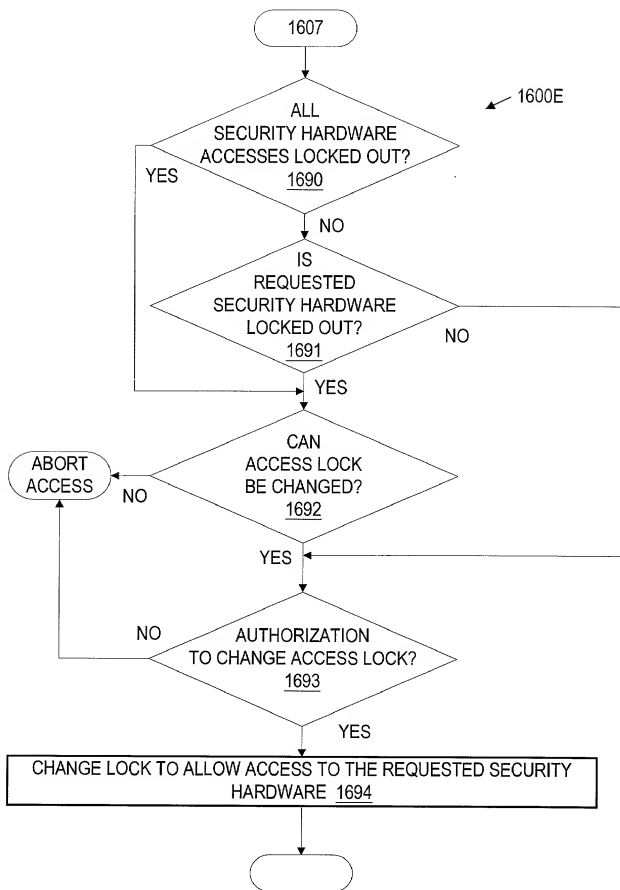


Fig. 16E



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1600F

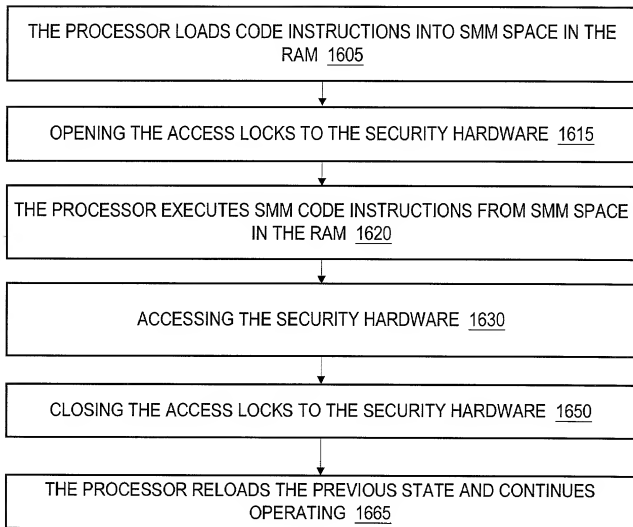


Fig. 16F

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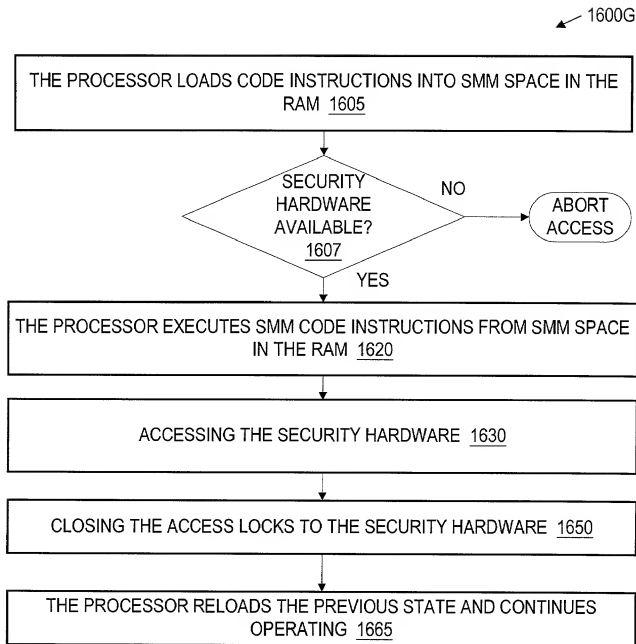
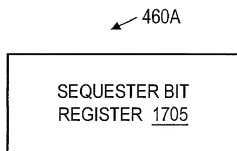


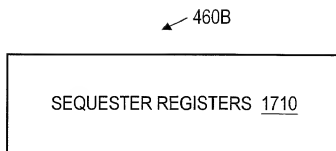
Fig. 16G

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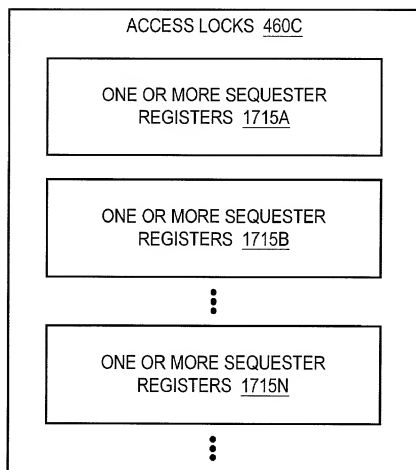
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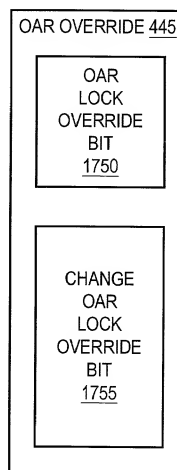
**Fig. 17A**



**Fig. 17B**



**Fig. 17C**



**Fig. 17D**



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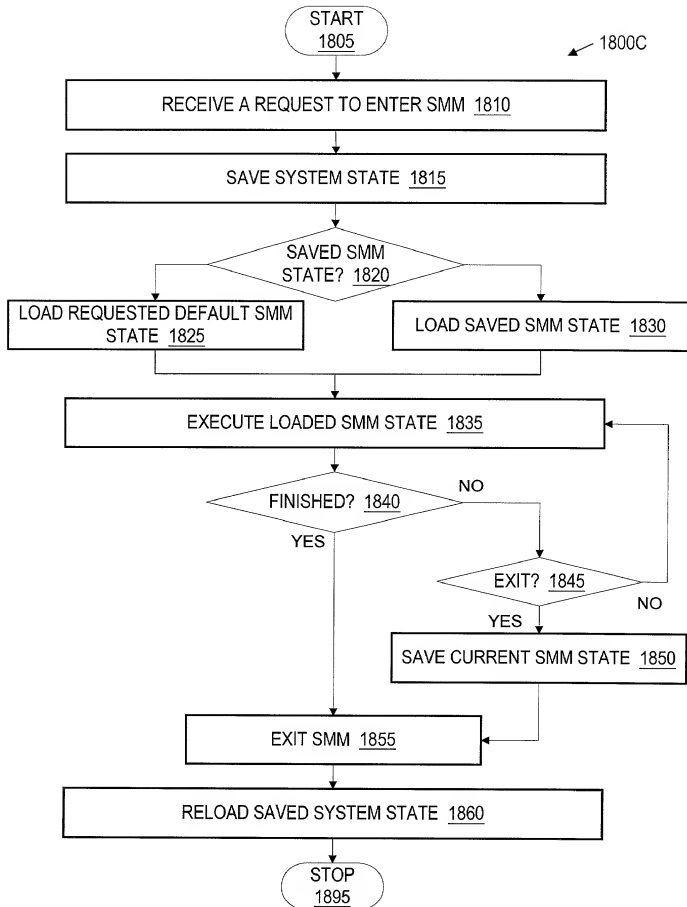


Fig. 18C

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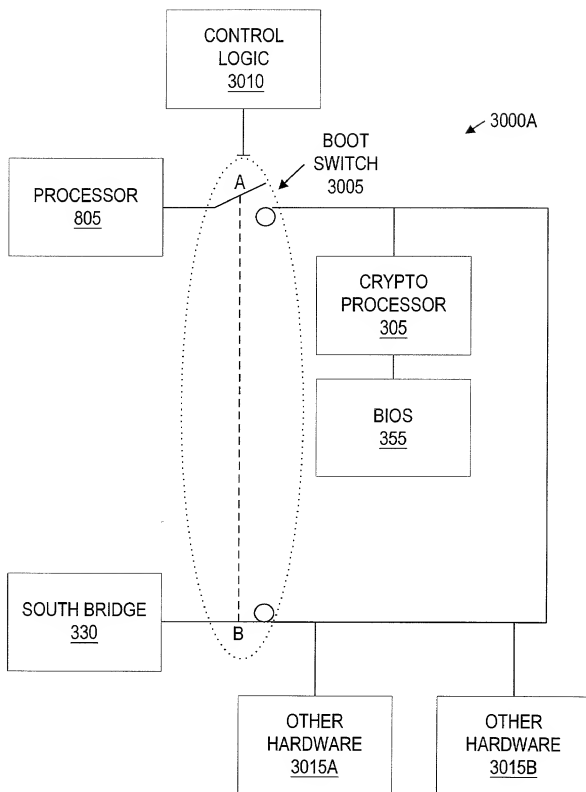
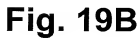


Fig. 19A



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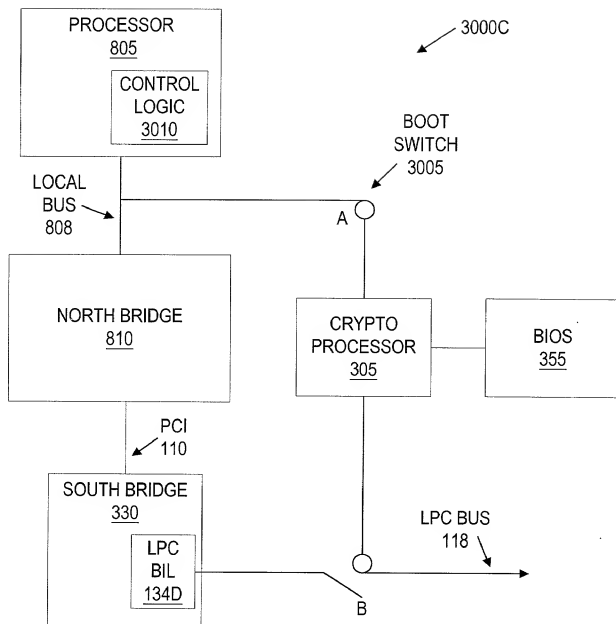
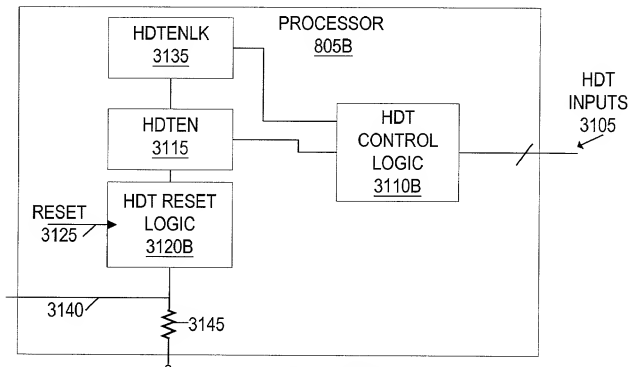


Fig. 19C



**Fig. 20B**



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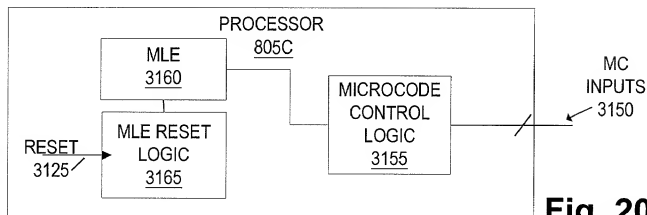


Fig. 20C

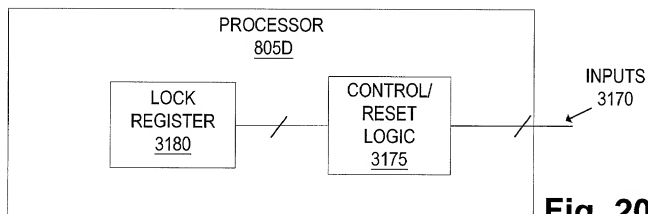
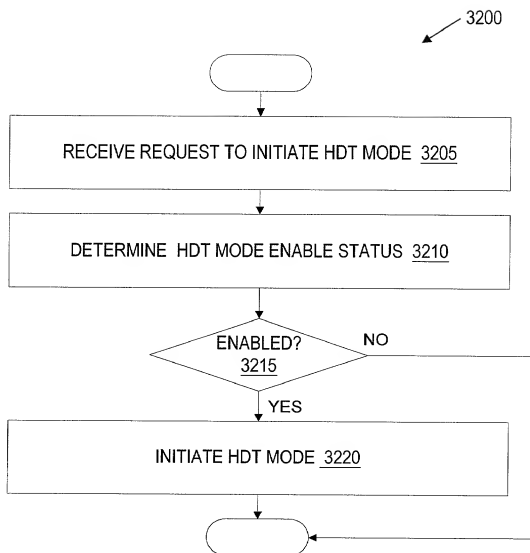


Fig. 20D

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**Fig. 21**

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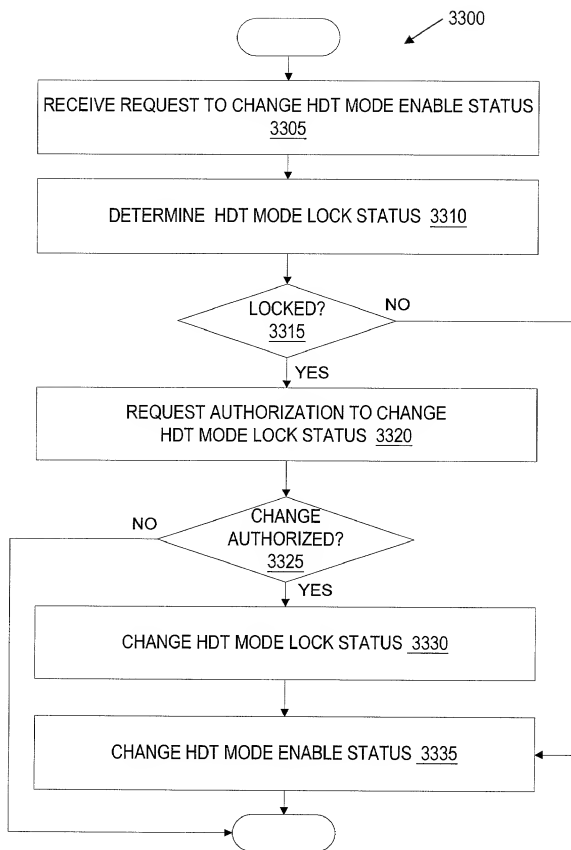
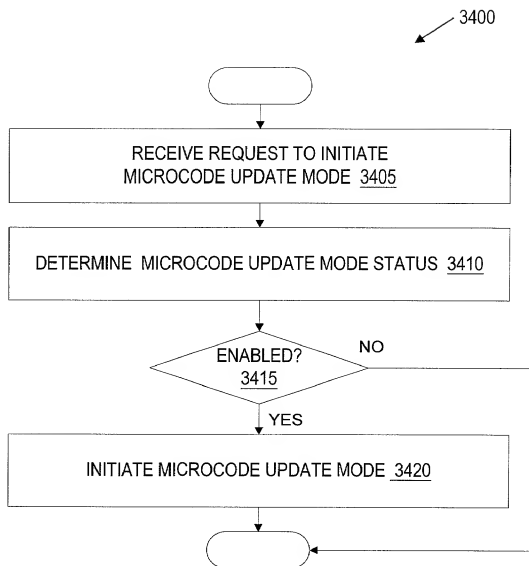


Fig. 22

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**Fig. 23**

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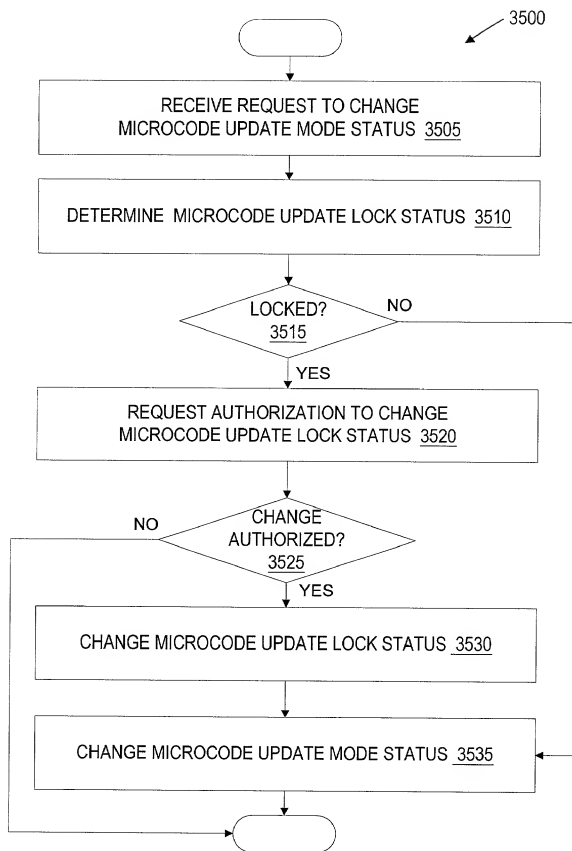


Fig. 24

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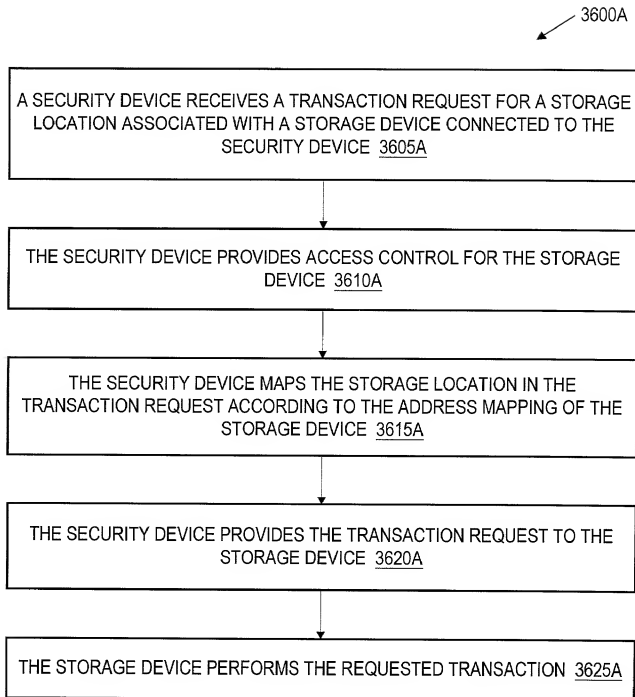


Fig. 25A

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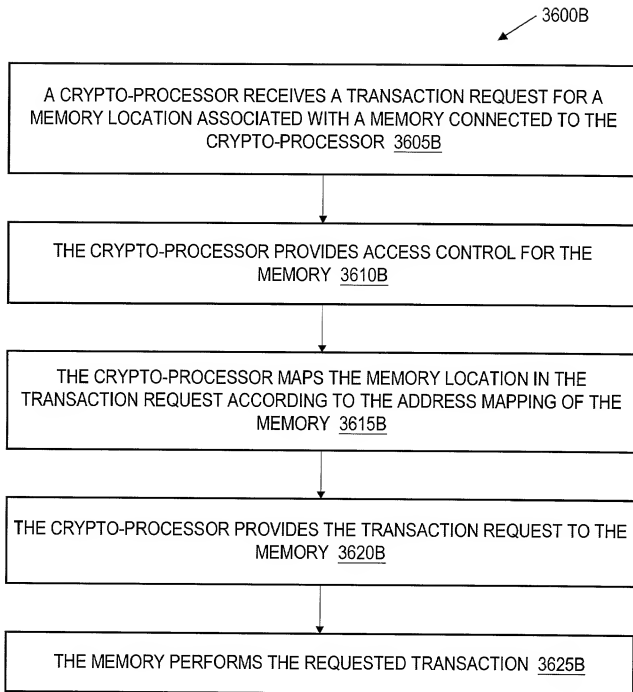


Fig. 25B



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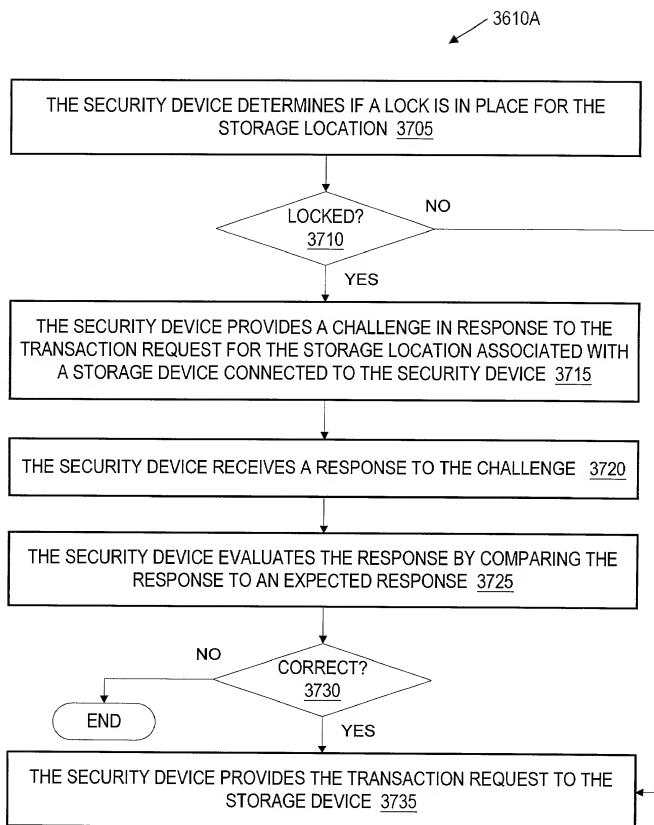
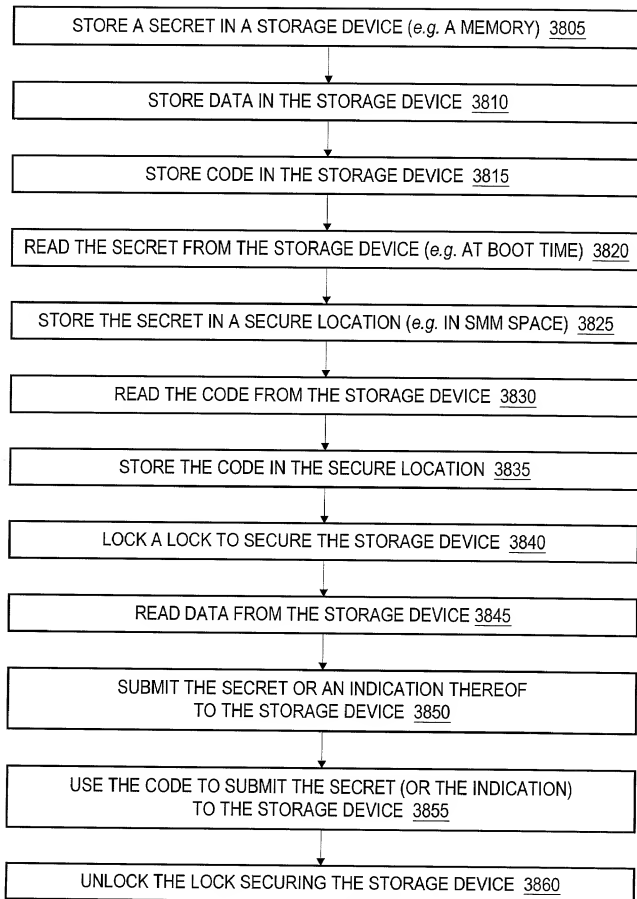


Fig. 26

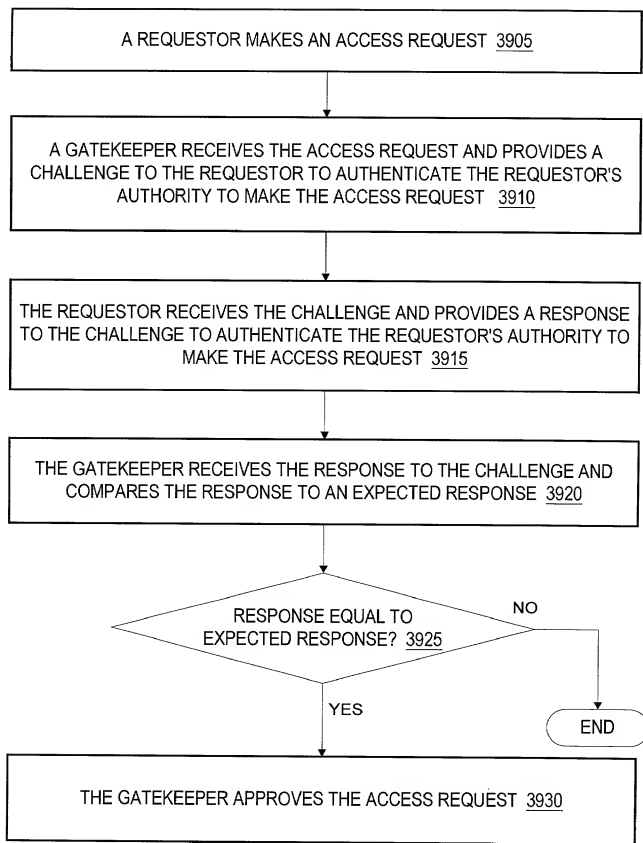
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3620

**Fig. 27**

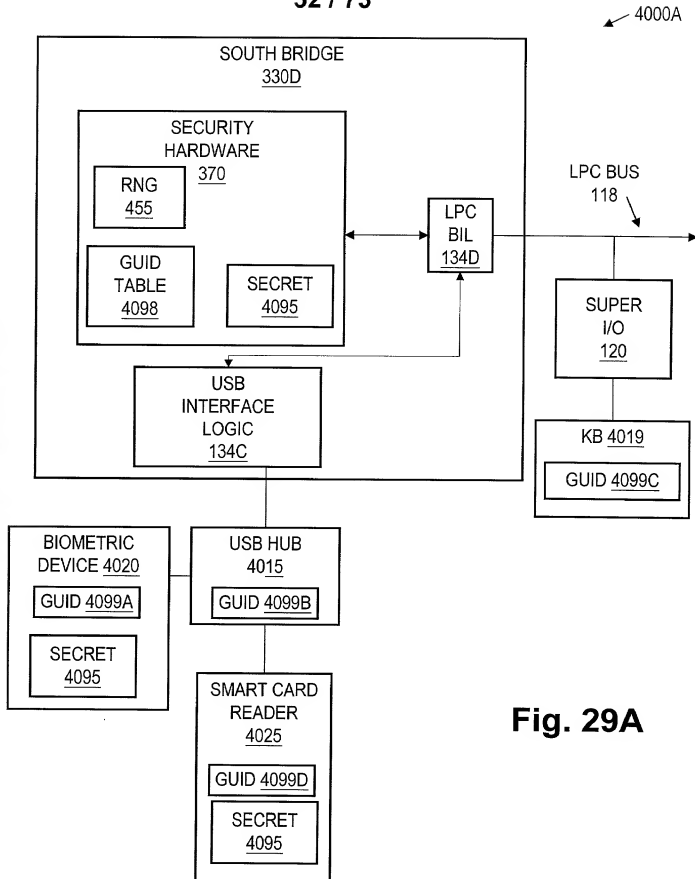
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3900



**Fig. 28**  
**(Prior Art)**

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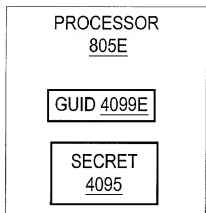


Fig. 29B

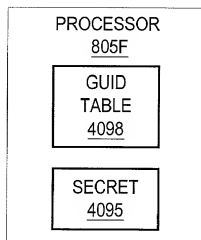


Fig. 29C

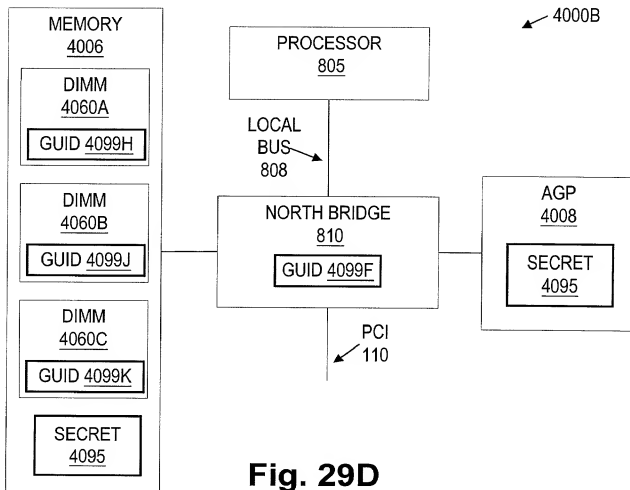


Fig. 29D

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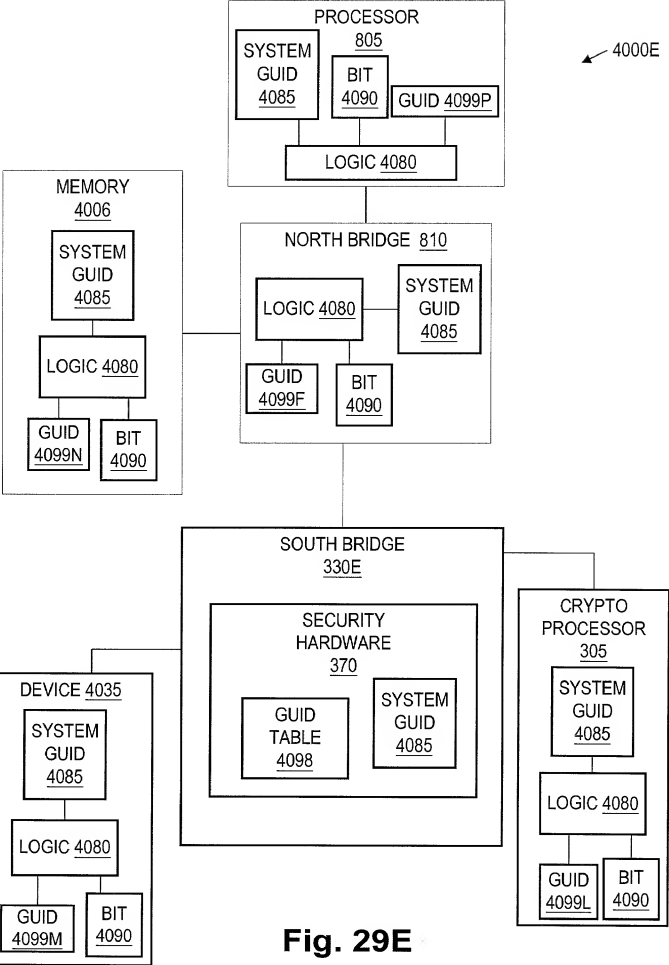


Fig. 29E

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4100A

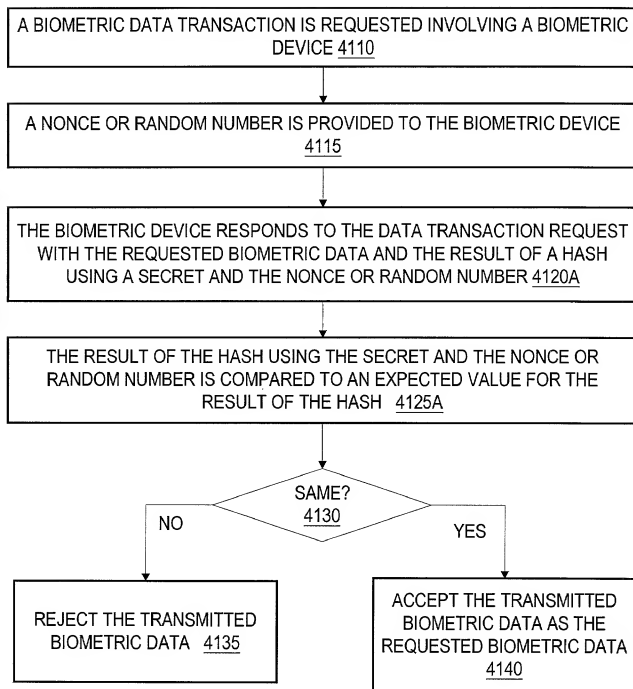


Fig. 30A

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4100B

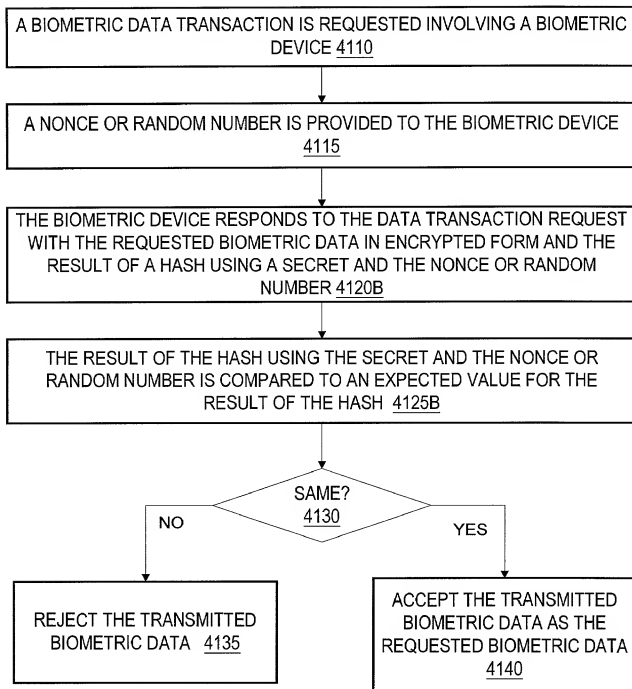
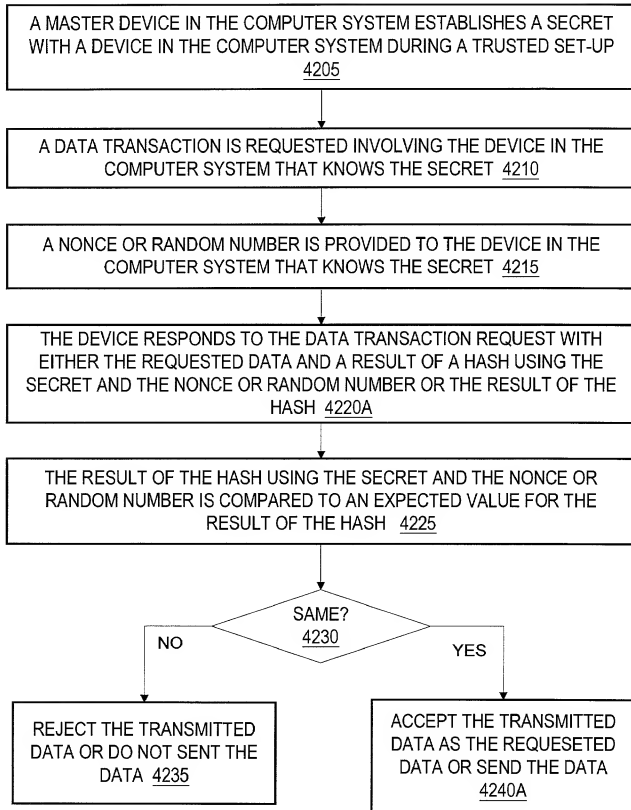


Fig. 30B





**Fig. 31A**

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4200B

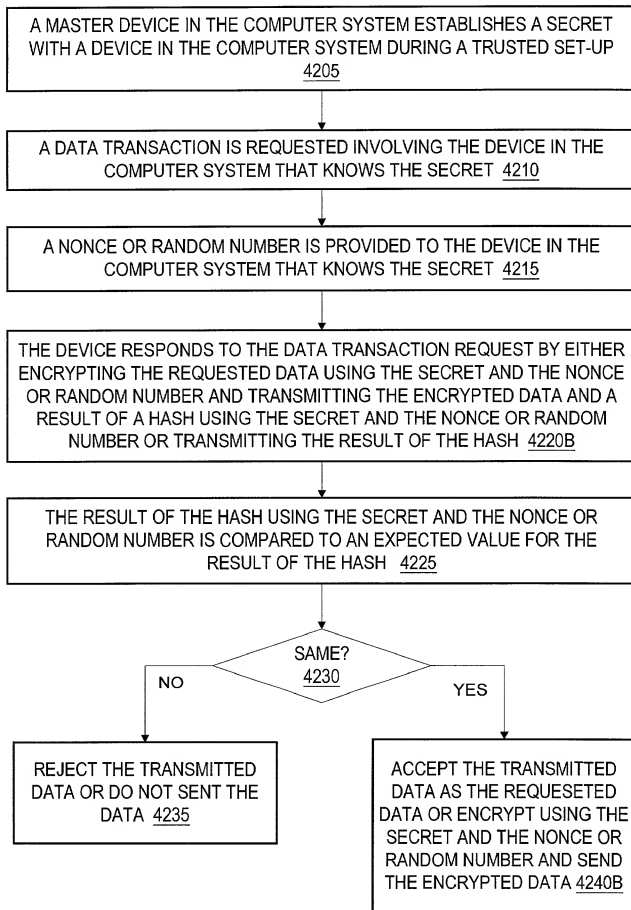
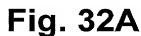


Fig. 31B

4300A



**Fig. 32A**

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4300B

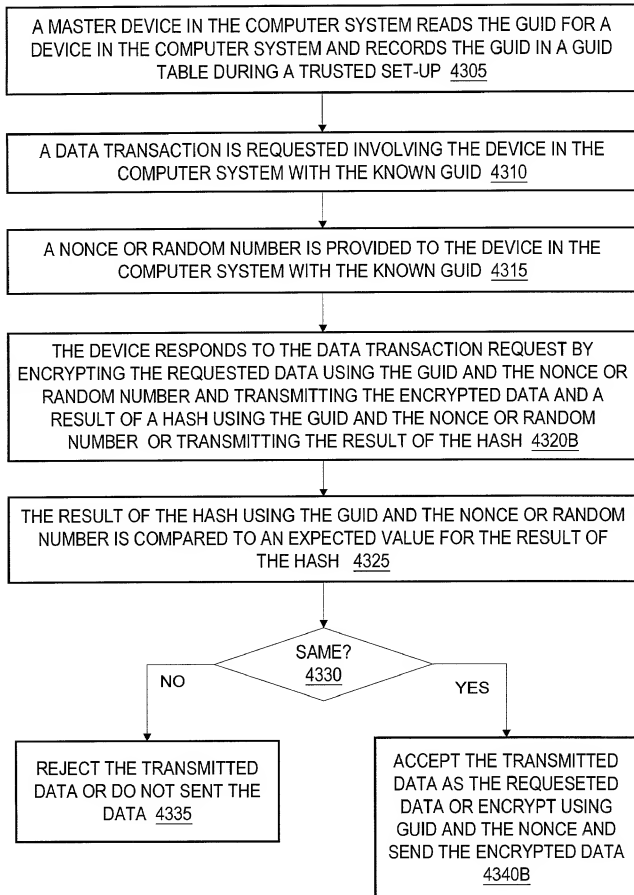


Fig. 32B

4300C



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4400

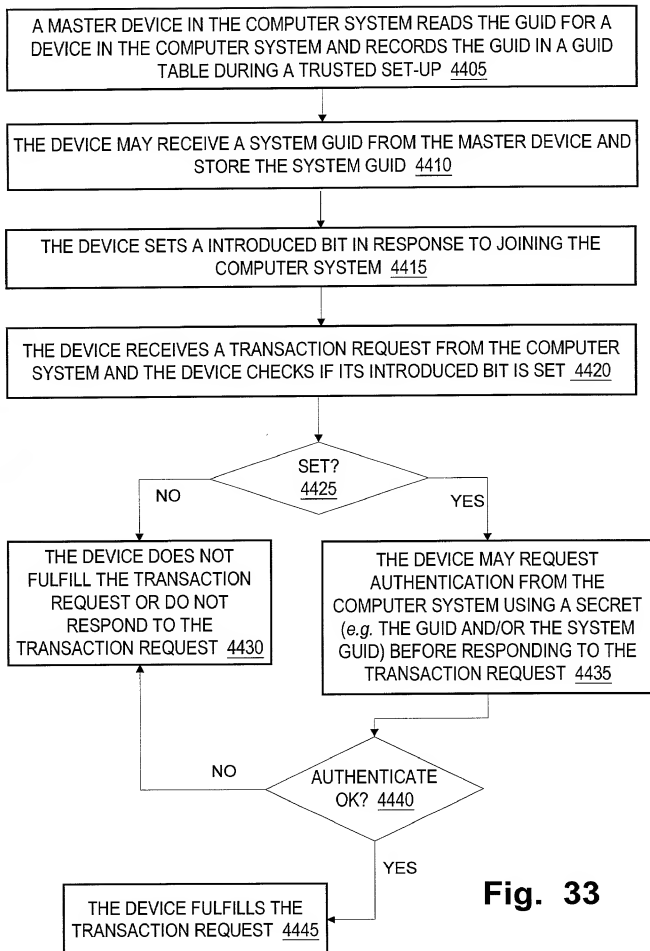


Fig. 33

4500





**Fig. 36**



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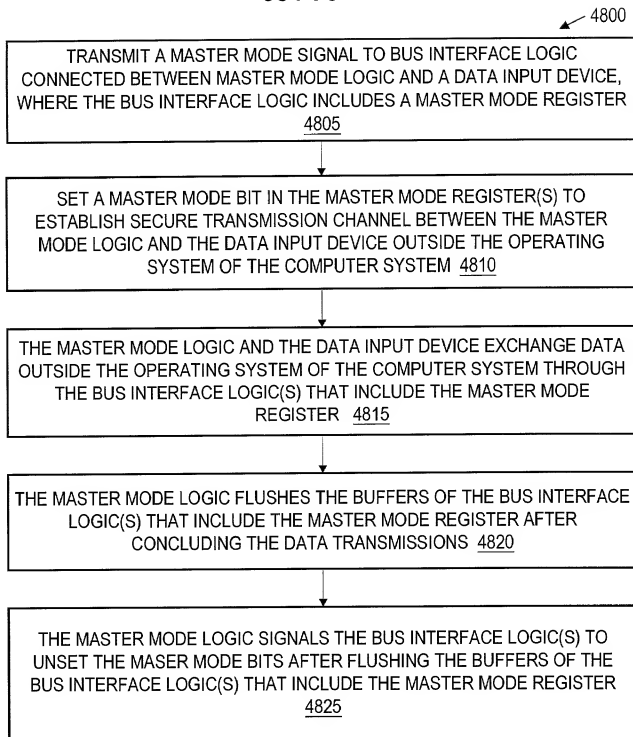


Fig. 37

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4900A

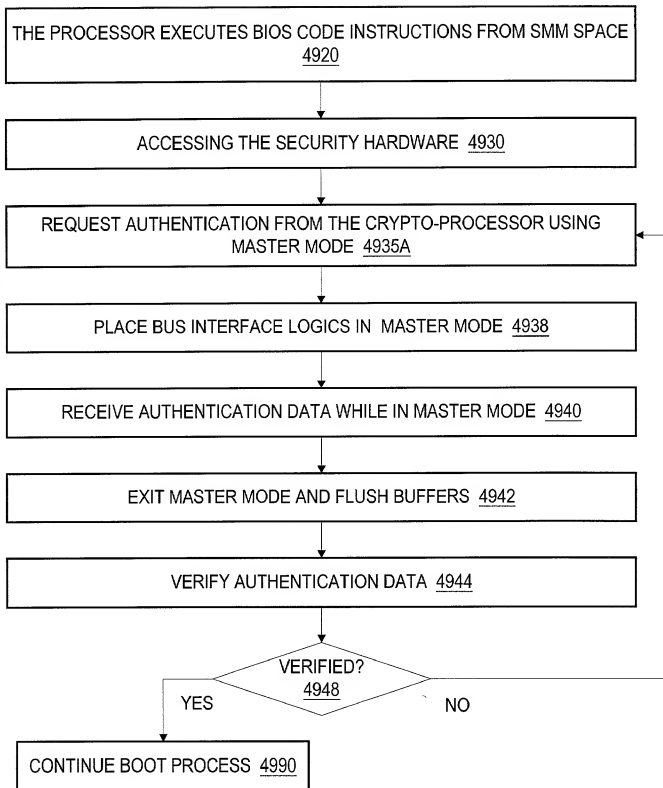


Fig. 38A

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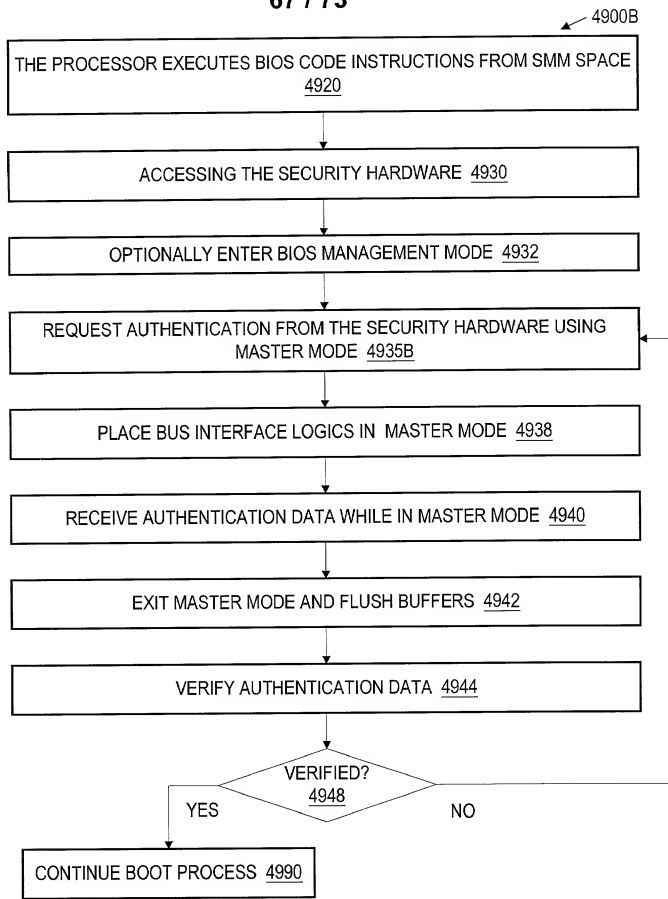
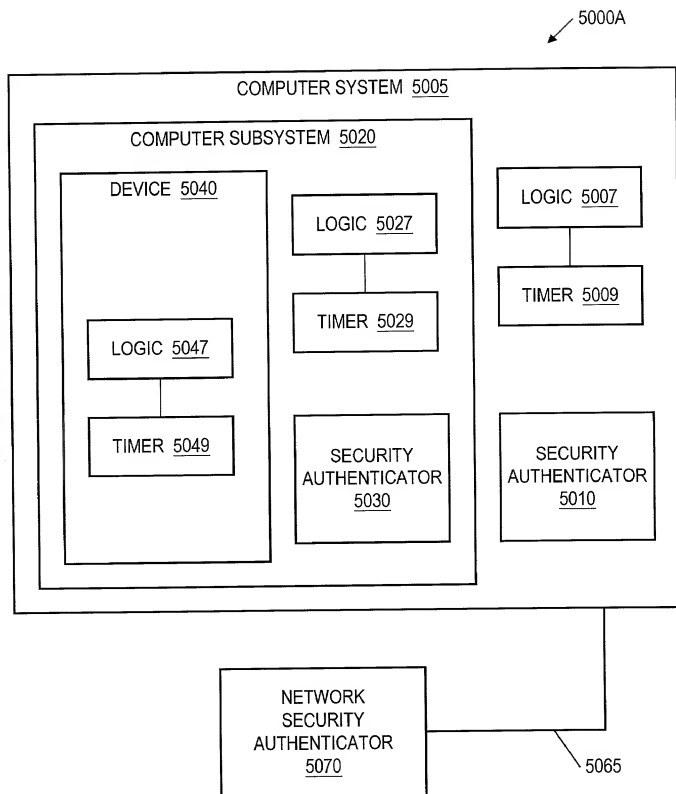
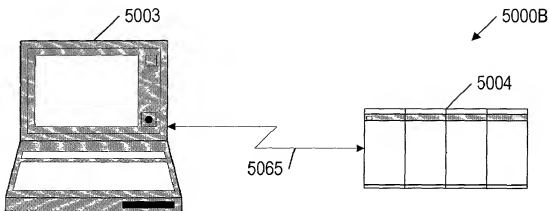


Fig. 38B

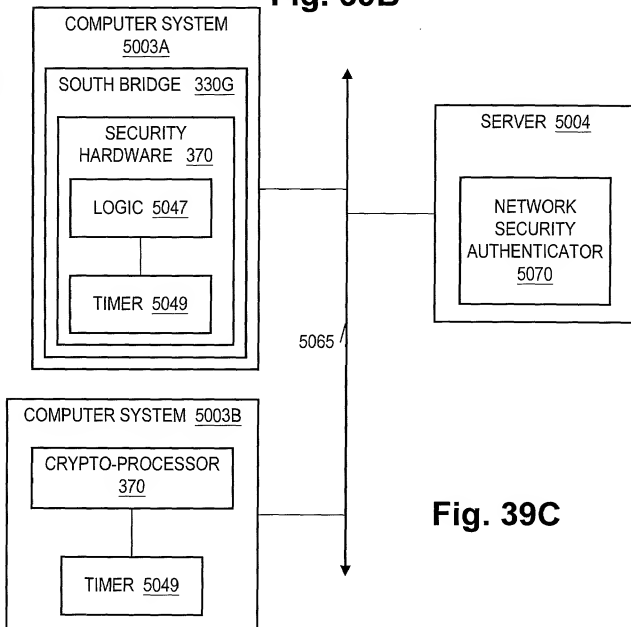


**Fig. 39A**

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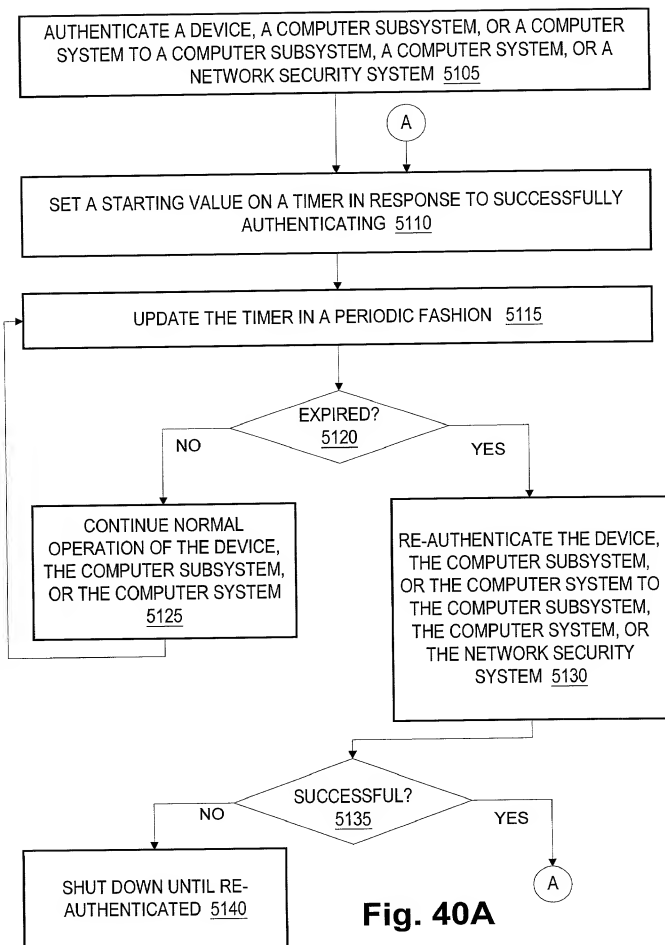


**Fig. 39B**

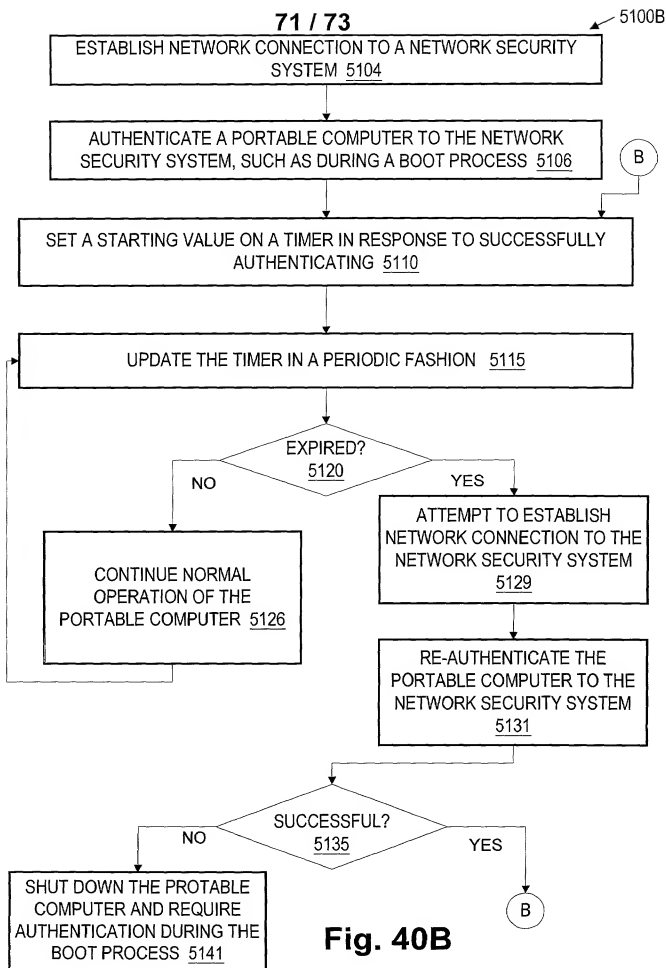


**Fig. 39C**

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**Fig. 40A**



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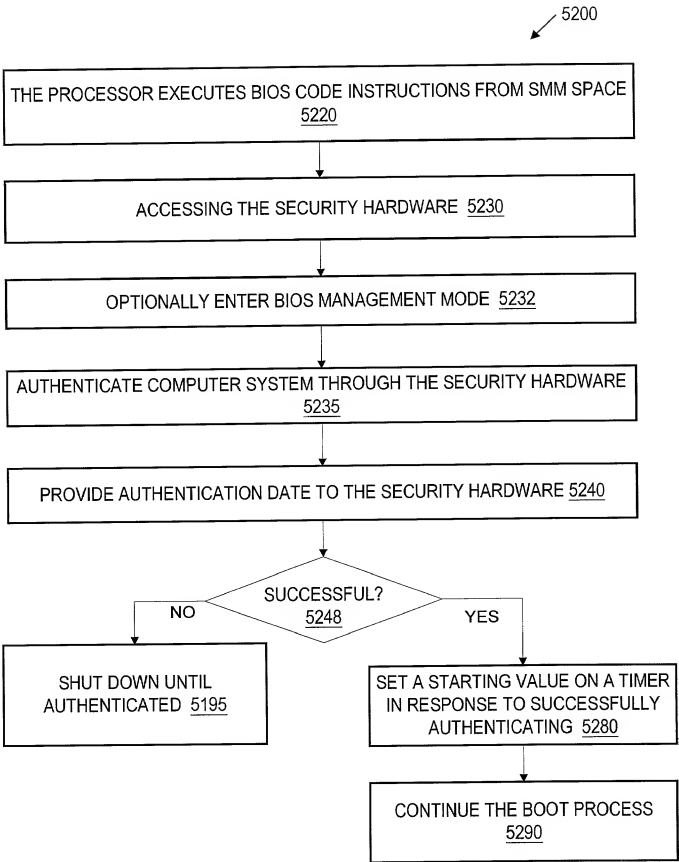


Fig. 41



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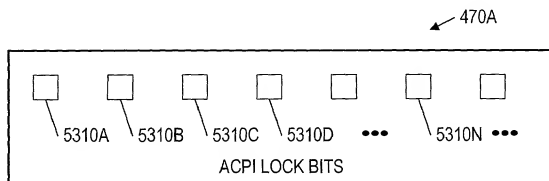


Fig. 42A

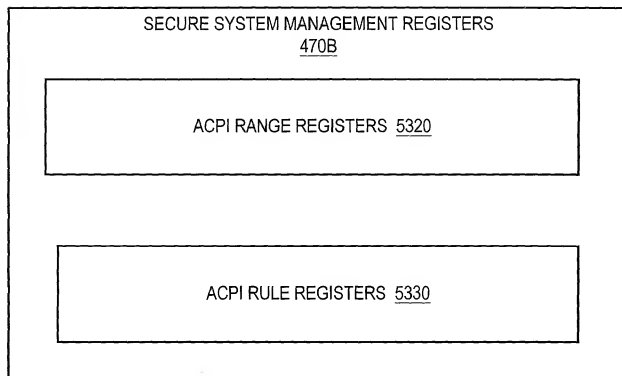


Fig. 42B

00853225-051101